Remarks

Claims 9-16 are pending in the application and are presented for reconsideration. Claims 9 and 15 have been amended; and claims 10-14 remain in the application unchanged. No new matter has been added.

Claim Rejections

Claim 9 is rejected under 35 U.S.C. § 102(e) as being anticipated by Mokovic et al. (US 2003/0107421).

Claims 10-14 and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Mokovic et al. (US 2003/0107421).

The Examiner's rejections of the claims are respectfully traversed.

Response to Rejections of Claims Under 35 U.S.C. § 102

a. Claims 9-14

The Examiner cites Mokovic as anticipating Applicant's claim 9. In particular, the Examiner states that "Figure 1 shows an input signal (80), a first pass gate (20), a master clock signal (CN), a first storage node (output of the transistor 20), a second pass gate (30), a slave clock (CP), a first inverter (120), a third pass gate (bottom transistor of passing gate 30), a second storage node (output of the transistor 30) as called for in claim 9."

Claim 9 recites:

> A circuit, comprising;
> an input conveying an input signal;
> a first pass gate coupled to the input and enabling a first signal in response to the input signal and in response to a master clock signal generating a clock signal;
> a first storage node coupled to the first pass gate and storing the first signal;
> a second pass gate connected to the first storage node and enabling a second signal in response to the first signal stored in the first storage node and in response to a slave clock signal, wherein the slave clock is a compliment to the master clock signal;
> a first inverter coupled to the first storage node and generating a first inverted signal in response to the first signal stored in the first storage node;

a third pass gate coupled to the first inverter and enabling a third signal in response to the first inverted signal and in response to the slave clock signal; and

an unclocked second storage node coupled to the second pass gate and coupled to the third pass gate, the second storage node storing the second signal and the third signal.

An important feature of Applicant's invention as recited in Claim 1 is the protection it offers during power-up of the circuit. As stated in the Applicant's specification at page 11, paragraph [0035], during power-up the state of the slave clock (310, 316) is indeterminate for some time and may remain low for an extended period. If the slave clock (310, 316) remains low for some time period, inverter (317) and inverter (319) will very rapidly settle to a stable state that will drive opposite (i.e., differential) values on the outputs. This protects downstream circuits that may be sensitive to non-differential inputs.

This protection feature of Applicant's invention is a result of the fact that the storage nodes are unclocked. That is, regardless of the states of the clock signals (master clock 304 and slave clock 310, 316), the values of the second and third signals will always rapidly settle to complimentary states, thereby protecting downstream circuitry that is sensitive to non-differential inputs.

In contrast, as shown in FIG. 1 in Mokovic, the inverters 40 and 110 that make up the allegedly equivalent "first storage node" are each clocked by the slave clock (CP), and the inverters 50 that make up the allegedly equivalent "second storage node" are each clocked by the master clock (CN). Thus, during power up, the master clock (CN) and slave clock (CP) may both remain low for an extended time period. This will result in an indeterminate value on the outputs of the second pass gate (30) and the third pass gate, which may adversely affect downstream circuits that may be sensitive to non-differential inputs. Accordingly, since Mokovic does not teach or suggest the feature of using *unclocked* storage nodes, Mokovic's circuit does not guarantee protection of downstream circuits that are sensitive to differential outputs.

For the reasons just described, Mokovic does not teach or suggest "an unclocked second storage node coupled to the second pass gate and coupled to

the third pass gate, the second storage node storing the second signal and the third signal" as required by Applicant's recited Claim 1.

Since Mokovic does not meet each and every limitation of Applicant's claim 1, per *Verdegaal Bros., Inc., supra*, Mokovic cannot be used in formulating an anticipation rejection under 35 U.S.C. § 102.

Furthermore, Mokovic cannot be used in formulating a 35 U.S.C. § 103 rejection of Applicant's claim 9. It has been established that "[i]f [the cited reference] does in fact teach away from [Applicant's invention], then that finding alone can defeat [an] obviousness claim." (annotation added) *Winner International Royalty Corp. v. Wang*, 53 USPQ2d 1580, 1587 (Fed. Cir. 2000). A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant . . . [or] if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant." *In re Gurley*, 27 F.3d 551, 553, 31 USPQ2d 1130, 1131 (Fed. Cir. 1994). In addition, if when combined, the references "would produce a seemingly inoperative device," then they teach away from their combination. *Tec Air*, 52 USPQ2d at 1298 (citing *In re Sponnoble*, 405 F.2d 578, 587, 160 USPQ 237, 244 (CCPA 1969)); *See also In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (finding no suggestion to modify a prior art device where the modification would render the device inoperable for its intended purpose).

Mokovic cannot be used in formulating a 35 U.S.C. § 103 rejection of Applicant's claim 9 because to remove the clocked nature of the inverter (40) in Mokovic would be to render the circuit inoperable for its intended function, namely as a "low-energy master-slave latch pair flip-flop" (*see* Mokovic, column 1, paragraph 4). Mokovic admits this in describing the flip-flop architecture 130, shown in FIG. 2 of Mokovic. As stated in Mokovic at col. 4, paragraph 4, "pull-up transistors of inverters 90, 120 of FIG. 1 are removed, leaving NMOS transistors, to save energy. However, *non-interrupted feedback inverters 140, 150 cause*

excessive short-circuit energy consumption and a longer time delay arising from a contention with the transmission-gates 160, 170." Thus, a removal of the clocked nature of the inverter (50) in Mokovic's Figure 1 *would render the circuit inoperable for its intended function of providing a low-energy circuit.*

Accordingly, Mokovic cannot even be used in formulating a 35 U.S.C. § 103 rejection of Applicant's claim 9.

In summary, none of Mokovic, Japanese Patent 5-37305, Chalasani, Shikata, or any of the other prior art of record, taken either alone or in any combination, meets each and every limitation of Applicant's claim 9. Per *Verdegaal Bros., Inc., supra*, therefore none of Mokovic, Japanese Patent 5-37305, Chalasani, Shikata, or any of the other prior art of record can be used in formulating an anticipation rejection under 35 U.S.C. § 102. Furthermore, since none of Mokovic, Japanese Patent 5-37305, Chalasani, Shikata, or any of the other prior art of record, taken in any combination, teach the essential limitation "an unclocked second storage node coupled to the second pass gate and coupled to the third pass gate, the second storage node storing the second signal and the third signal", Mokovic, Japanese Patent 5-37305, Chalasani, Shikata, or any of the other prior art of record, cannot even be combined to formulate an obvious-type rejection under 35 U.S.C. § 103. Accordingly, Applicant respectfully submits that the rejection of claim 9 should be withdrawn and that claim 9 is now in position for allowance.

Claims 10-14 each depend from independent base claim 1 and add further limitations. For at least the same reasons that Claim 1 is not shown, taught, or disclosed by the cited references, Claims 2-10 are likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of claims 2-10 should be withdrawn.

b. Claims 15-16

Amended claim 15 recites:

> A method of operating a differential register, the differential register comprising a first pass gate having a first pass gate data input, a first pass gate enable input, and a first pass gate output; a first storage node coupled to the first pass gate output; a second pass gate having a second

pass gate data input connected to the first storage node and the first pass gate output, a second pass gate enable input, and a second pass gate output; a first inverter having a first inverter input connected to the first storage node and the first pass gate output and a first inverter output; a third pass gate having a third pass gate data input coupled to the first inverter output, a third pass gate enable input, and a third pass gate output; an output node, and a complimentary output node, the method comprising the steps of:

receiving a data input signal on the first pass gate data input and a master clock signal on the first pass gate enable input;

conveying the data input signal from the first pass gate data input to the first pass gate data output and storing the data input signal in the first storage node when the master clock signal is in a first master clock signal state;

receiving the stored data input signal on the second pass gate input and a slave clock signal on the second pass gate enable input;

conveying the stored data input signal from the second pass gate data input to the second pass gate data output for storage in the second storage node when the slave clock signal is in a first slave clock signal state, wherein the slave clock signal is a compliment to the master clock signal;

inverting the stored input data signal to generate an inverted stored input data signal;

receiving the inverted stored data input signal on the third pass gate input and the slave clock signal on the third pass gate enable input;

conveying the inverted stored data input signal from the third pass gate data input to the third pass gate data output for storage in the second storage node when the slave clock signal is in the first slave clock signal state; and

on power-up, conveying the stored data input signal stored in the second storage node out of the output node and conveying the inverted stored data input signal stored in the second storage node out of the complimentary output node regardless of states of the master clock signal and the slave clock signal.

Claim 15 recites limitations similar to Claim 1, including "on power-up, conveying the stored data input signal stored in the second storage node out of the output node and conveying the inverted stored data input signal stored in the second storage node out of the complimentary output node *regardless of states of the master clock signal and the slave clock signal*". For at least the same reasons that Claim 1 is not shown, taught, or disclosed by the cited references,

Claim 15 is likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of Claim 15 should be withdrawn.

Claim 16 depends from independent base claim 15 and add further limitations. For at least the same reasons that Claim 15 is not shown, taught, or disclosed by the cited references, Claim 16 is likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of Claim 16 should be withdrawn.

Conclusion

In view of the foregoing remarks, it is respectfully submitted that none of the references cited by the Examiner taken alone or in any combination shows, teaches, or discloses the claimed invention, and that Claims 9-16 are in condition for allowance. Reexamination and reconsideration are respectfully requested.

Should the Examiner have any questions regarding this amendment, or should the Examiner believe that it would further prosecution of this application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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Jessica Costa

Jessica Costa, Reg. No. 41,065

The Law Offices of Jessica Costa, PC
P.O. Box 460 Crozet, VA
22932-0460
(434) 823-2232
(434) 823-2242 (fax)